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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MARTINEZ, DAVID E	

ART UNIT	PAPER NUMBER
2182	7

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,135	JAHNKE ET AL.	
	Examiner	Art Unit	
	David E Martinez	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-12* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9 and 12, are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,754,884 to Swanstrom.

1. With regards to claim 1, Swanstrom teaches a data transfer system comprising:

a plurality of bus devices, at least one bus device being a bus data supplying device capable of supplying data, at least one bus device being a bus data receiving device capable of receiving data and at least one bus device being a bus master device capable of requesting and controlling data transfer [column 6 lines 1-15];

a data bus connected to each of said plurality of bus devices and capable of transferring data from a bus data supplying device to a bus data receiving device under control of a bus master device [column 6 lines lines 1-15];

a direct memory access unit connected to said data bus as a bus master device [figs 7, 8, column 8 lines 51-57], said direct memory access unit including:

a source word size register storing a source word size [fig 8, element 870 column 9 lines 7-20],

a target word size register storing a target word size [fig 8, element 870 column 9 lines 7-20],

a source start address register storing a source start address [fig 8, element 804],

a source increment size register storing a source increment size [fig 8, element 808],

a target start address register storing a target start address [fig 8, element 806],

a target increment size register storing a target increment size [fig 8, element 810],

said direct memory access unit capable of transferring data from a first bus data supplying device to a first bus data receiving device via said first bus by recalling data from a first bus data supplying device beginning at said source start address and thereafter at successive addresses differing by said source increment size in a data size corresponding to said source word data size and supplying said recalled data to a first bus data receiving device beginning at said target start address and thereafter at successive addresses differing by said target increment size in a data size corresponding to said target word size [column 6 lines 1-15, column 8 line 51 to column 9 line 43].

2. With regards to claim 2, Swanstrom teaches the data transfer system of claim 1, wherein: said direct memory access unit further includes

a read data register loaded with data from said bus data supplying device via said data bus in said source word size [column 9 lines 21-26],

a write data register supplying data to said bus data receiving device via said data bus in said target word size [column 9 lines 21-26], and

a word formatter connected to transfer data from said read data register to said write data register thereby aligning data in said target word size in said write data register [inherently part of the dma when buffering data from a source whose word size differs from the word size of

the destination. The data must be follow a certain format for the avoidance of data corruption during a data transfer].

3. With regards to claim 3, Swanstrom teaches the data transfer system of claim 2, further comprising:

at least one first bus device being a first bus supplying/receiving device capable of both supplying data to said first bus and receiving data from said first bus [column 6 lines 1-15].

4. With regards to claim 4, Swanstrom teaches the data transfer system of claim 3, wherein: at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer [column 6 lines 1-15].

5. With regards to claim 5, Swanstrom teaches the data transfer system of claim 3, wherein: at least one first bus supplying/receiving device consists of a direct memory access unit which is further capable of controlling data transfer [column 6 lines 1-15].

6. With regards to claim 6, Swanstrom teaches the data transfer system of claim 3, wherein: at least one first bus supplying/receiving device consists of a memory which is not capable of controlling data transfer [column 6 lines 1-15].

7. With regards to claim 7, Swanstrom teaches the data transfer system of claim 3, wherein: at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer, said central processing unit connected to said direct memory access unit for loading data into said source data size register and into said target data size register [column 6 lines 1-15, column 8 line 51 to column 9 line 43].

8. With regards to claim 9, Swanstrom teaches the data transfer system of claim 1, wherein: at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer, said central processing unit connected to said direct memory access unit for loading data into said source start address register, said

source increment size register storing, said target start address register and said target increment size register [column 6 lines 1-15, column 8 line 51 to column 9 line 43].

9. With regards to claim 12, Swanstrom teaches the data transfer system of claim 1, wherein said plurality of bus devices consist of first bus devices and said data bus consists of a first data bus [column 6 lines 1-15], said data transfer system further comprising:

a plurality of second bus devices, at least one second bus device being a second bus data supplying device capable of supplying data, at least one second bus device being a second bus data receiving device capable of receiving data and at least one second bus device being a second bus master device capable of requesting and controlling data transfer, each second bus device having a predetermined data size [column 8 lines 1-13, column 9 lines 7-20];

a second data bus having said predetermined data size connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device[column 8 lines 1-13, line 51 to column 9 line 43];

a bus bridge [fig 7 element 792] connected to said first data bus [fig 7 element 730] and said second data bus [fig 7 element 794], said bus bridge capable of transferring data between said first bus devices and said second bus devices [column 7 lines 63-67]; and

wherein said direct memory access unit stores said predetermined data size in said source word size register [fig 8, element 870 column 9 lines 7-20] for data transfer from a second bus device to a first bus device via said bus bridge and stores said predetermined data size in said target word size register [fig 8, element 870 column 9 lines 7-20] for data transfer from a first bus device to a second bus device via said bus bridge [column 8 line 51 to column 9 line 43].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,754,884 to Swanstrom in view of US Patent No. 6,115,767 to Hashimoto et al (Hashimoto).

11. With regards to claim 10, Swanstrom fails to teach the limitations of claim 10, however Hashimoto teaches a data transfer system comprising:

a bus arbiter (figs 1, 2, element 9) connected to each of at least one bus master device (fig 1, element 401), a direct memory access unit (figs 1, 2, element 11) and a first bus (figs 1, 2, element 406), the bus arbiter granting control of data transfer on the data bus to one and only one bus master device (column 4, lines 39-50); and

the direct memory access unit further includes

a counter value register storing a number of data words to be transferred by the direct memory access unit (fig 2, element 2, column 5, lines 14-20),

a block size register storing a block size to be transmitted without interruption (fig 2, element 3, column 5, lines 14-20),

the direct memory access unit requesting bus control from a bus arbiter (column 4, lines 39-50) and upon grant of control of data transmission on said data bus, said direct memory access unit thereafter

transferring data in an amount equal to the lesser of said number of data words to be transferred and said block size to be transmitted without interruption,

thereafter

ending data transfer if data transferred equals said number of data words to be transmitted, and

suspending data transfer, releasing control of data transfer on said data bus and re-requesting bus control from said bus arbiter (column 5, line 66 to column 6, line 25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Swanstrom with the teachings of Hashimoto by providing a bus controller, a counter value register, and a block size register such as disclosed Hashimoto, in order to improve overall system performance on the bus, by using DMA transfers that minimize CPU interaction that optimize pipelining of data burst transfers on the bus.

12. With regards to claim 11, Swanstrom teaches the data transfer system of claim 10, wherein:

at least one first bus supplying/receiving device consists of a central processing unit which is further capable of controlling data transfer, said central processing unit connected to said direct memory access unit [column 6 lines 1-15, column 8 line 51 to column 9 line 43]. As shown above, Swanstrom discloses the central processing unit loads all the necessary values into the DMA that are needed for it to do its data transferring.

Swanstrom fails to teach for loading data into said counter value register and said block size register because those are elements of the Hasimoto reference above.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the central processing unit load data into the counter value register and the block size

register since the DMA is controlled by the central processing unit in the first place for the same reasons as those disclosed above in claim 10.

Response to Arguments

Applicant's arguments with respect to claim 1 and dependent claims 2-7, and 9-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E Martinez whose telephone number is (703) 305-4890. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM

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